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(71) Applicant
Sharp Kabushiki Kaisha (Japan),
22-22 Nagaike-cho, Abeno-ku, Osaka, Japan

(72) Inventors
Hirohisa Tanaka,
Yutaka Takafuji,
Mitsuhiro Koden

(74) Agent and/or Address for Service
Boult, Wade & Tennant, 27 Furnival Street,
London EC4A 1PQ

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(58) Field of search
H1K

(54) Thin film transistor

(57) A thin film transistor comprises an insulating substrate 10 on which a gate electrode 20 is formed. A gate-insulating layer 30, 31 is formed on the gate electrode, a semiconductor layer 40 is formed on the gate-insulating layer and an insulating layer 90 is formed so as to cover the semiconductor layer and has two openings 91, 92 through which a source electrode 50 and a drain electrode 60 electrically contact the semiconductor layer.

Fig. 5

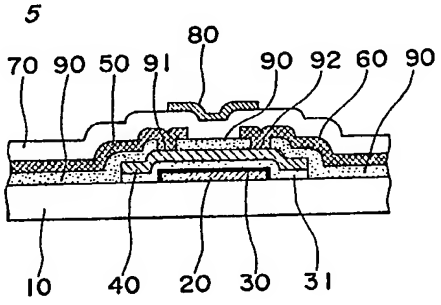

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Fig. 1

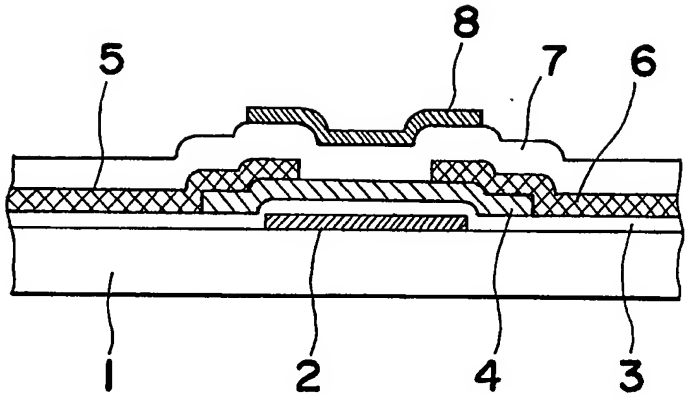


Fig. 2

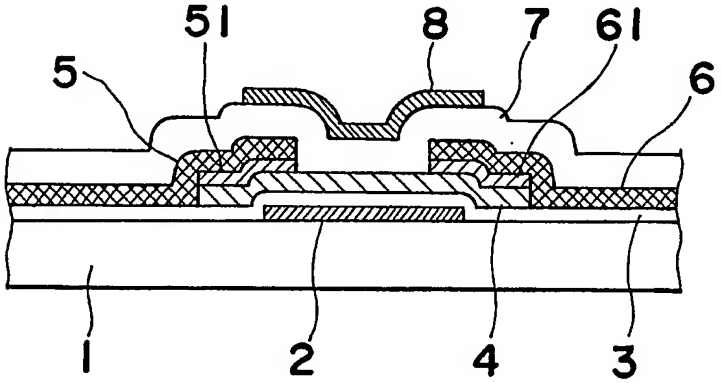


Fig. 3

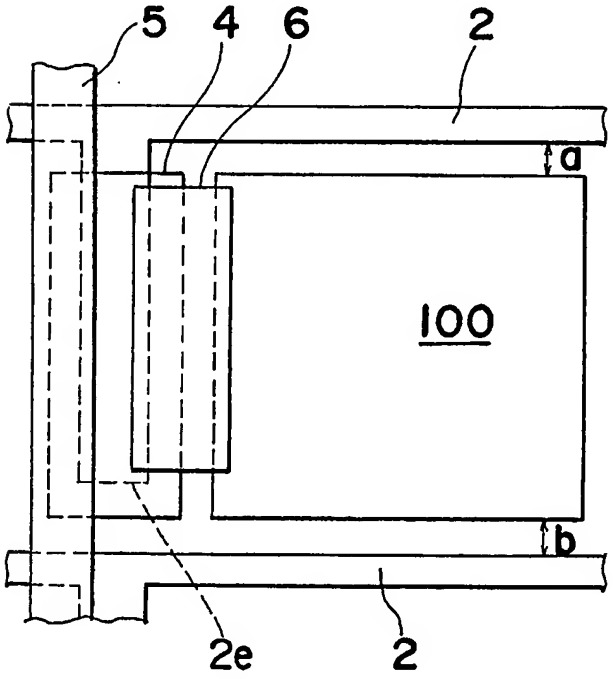


Fig. 4

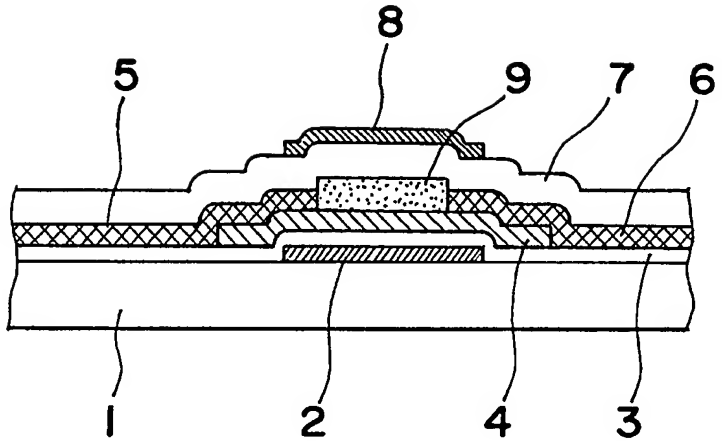


Fig. 5

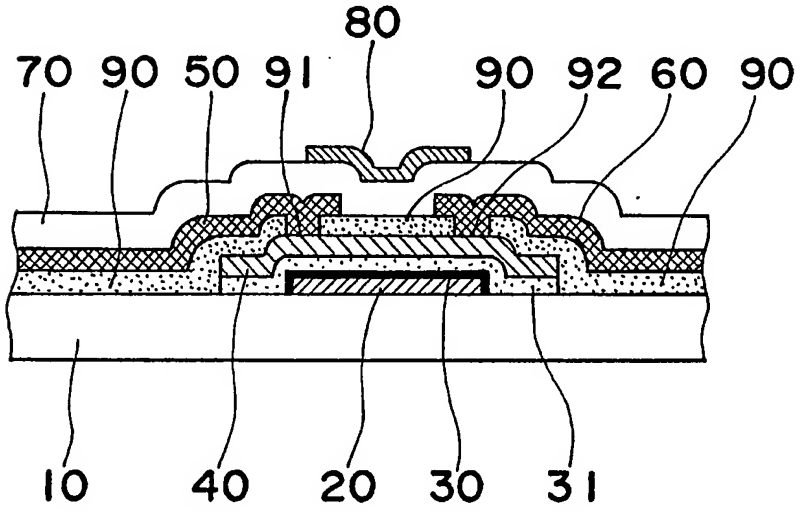


Fig. 6

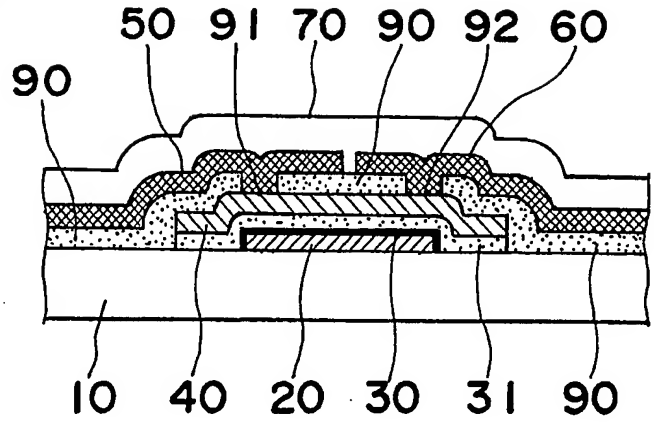


Fig. 7

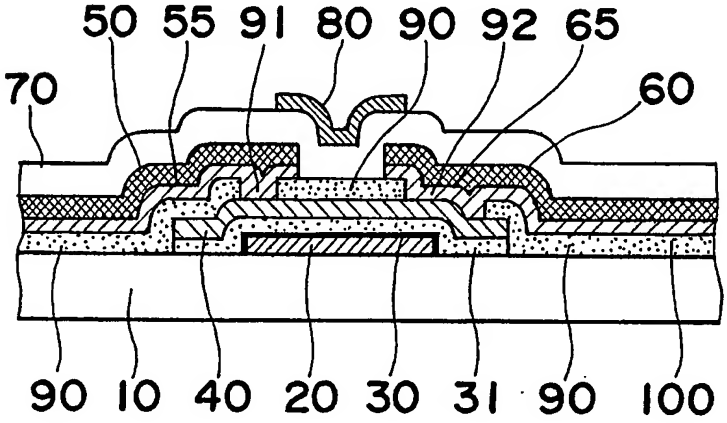
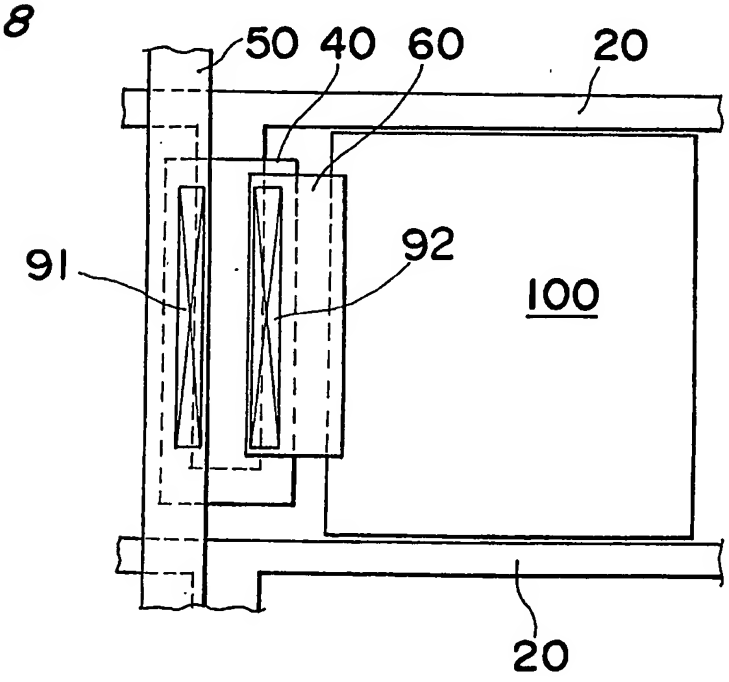


Fig. 8



SPECIFICATION

Thin film transistor

Field of the invention

The present invention relates to the structure of thin film transistor (hereinafter refered to as TFT).

Description of prior art

Figure 1 shows a general example of the prior art structure of TFT. The production process is as follows. A gate electrode 2, a gate-insulating film 3 and a semiconductor layer 4 are successively deposited on an insulating substrate 1. Then, a source electrode 5 and a drain electrode 6 are formed each on a part of the semiconductor layer 4 and the gate-insulating film 3. Furthermore, a passivation film 7 and a light shield 8 are deposited successively. For the insulating substrate 1, for example, a glass plate, a ceramic plate or a silica plate is used. The gate electrode 2 is made of a metallic material such as Al, Ni, Cr and Au, while the gate-insulating film 3 is made of an oxide or a nitride such as SiO, SiO_2, Al_2O_3, Ta_2O_5 and Si_3N_4. The semiconductor layer 4 is formed with a semiconducting material such as CdS, CdSe, Te, PbS, amorphous silicon (hereinafter refered to as a-Si) or microcrystalline silicon wherein at least a part of silicon becomes microcrystalline. The source and drain electrodes 5, 6 are made, for example, as an Al film or n^+ a-Si film. The passivation film 7 is made of an oxide or a nitride such as SiO_2 and Si_3N_4, while the light shield is made of a metallic material such as Al.

When the semiconductor layer 4 is made of a-Si, an Al film or multilayer film consisting of n^+ a-Si and a metallic material such as Ti is often used as the source and drain electrode 5, 6. Figure 1 shows an example of the structure of TFT in which Al electrodes are used. Figure 2 shows another example of the structure of TFT wherein n^+ a-Si layers 51 and 61 are each interposed between the semiconductor layer 4 and Ti films 5, 6, and each of multilayer electrodes consists of n^+ a-Si layer 51 and 61 and Ti film 5 and 6 respectively.

In such cases that Al film or multilayer film of a metallic material and n^+ a-Si is used for electrode material in the process of producing TFT of a-Si, following problems arise:

(1) If Al film is used for electrode material, the temperature of the substrate 1 is usually kept high on the deposition of Al from the standpoint of the adhesion strength of Al and the stability of the quality of Al film. Then, Al atoms deposited on the a-Si layer 4 migrate into the a-Si layer 4. Thus, Al atoms remains in the a-Si layer 4 after the patterning of the source and drain electrodes 5, 6 so that the short circuit between both electrodes 5, 6 or the deterioration of the a-Si layer is liable to occur.

On the contrary, if Al is deposited at a low temperature, the adhesion strength becomes weak and the quality of the deposited film becomes unstable.

(2) If a multilayer film consisting of n^+ a-Si and metal such as Ti is used for the source and drain electrodes 5, 6 as shown in Figure 2, the abovementioned contamination of the semiconductor layer 4 with Al atoms does not occur. It is necessary to etch the n^+ a-Si film 51 selectively against the a-Si semiconductor layer 4 in the process of the patterning of the n^+ a-Si film 51. However, both n^+ a-Si film 51 and a-Si semiconductor layer 4 are etched quite similarly to each other by an etchant such as ($HF+HNO_3$) mixed solution and CF_4 plasma. Then, the n^+ a-Si film on the a-Si semiconductor layer 4 should be etched selectively by controlling the etching time. Unfortunately, at present, the fluctuation in the thickness of n^+ a-Si film, the quality of n^+ a-Si film or the etching rate makes it difficult to control the process of producing a multilayer film so that the characteristics of TFT is inadequate for the stability and the reproducibility. Thus, in order to production a TFT of good characteristics it is required to establish the technique of etching n^+ a-Si film selectively.

(3) In a TFT with a structure shown in Figures 1 and 2, a fairly large electrical capacitance exists between the gate electrode 2 and the source and drain electrodes 5, 6, and affects the characteristics of TFT.

(4) If a plurality of TFT having a structure as shown in Figures 1 and 2 are used as addressing devices of a liquid crystal display apparatus of the matrix type, the active area to dead area ratio (A/D ratio), that is, the ratio between the area of the pixel electrodes and the remainder of the display becomes low due to the following reasons. Figure 3 shows an arrangement of a TFT and a pixel electrode in such a liquid crystal display apparatus. (For simplicity, such layers as the gate-insulating film 3 are omitted for clarity in Figure 3.) Gate electrodes 2 are formed parallel to each other and source electrodes 5 perpendicular to the gate electrodes 2. Near each intersection of gate electrodes 2 and source electrodes 5, a TFT is constructed with an extension 2e of the gate electrode 2 and a side part of the source electrode 5, and the drain electrode 6 is connected electrically to the corresponding pixel electrode 100 which is deposited on the gate-insulating film. The gate-insulating film should be thin enough between the gate electrode 2 and the semiconductor film 4 to obtain necessary TFT characteristics. Thus, the gate-insulating film is thin also in the area of pixel electrodes 100. If the gate electrodes 2 and the pixel electrodes 100 are formed close to or overlapped with each other, troubles such as the short-circuit through pin-holes in the gate-insulating film 3 and the interference of the signal of the gate electrode 2 with that of the pixel electrode 100 occur because the gate-insulating electrode is thin. Then, the gaps a, b between the gate electrodes 2 and the pixel electrodes 100 should be wide enough to prevent such troubles. This makes the area of the pixel electrode 100 smaller so that the A/D ratio is reduced.

In order to overcome the abovementioned problems (1) and (2), a TFT having a structure shown in Figure 4 was proposed and has been used practically. In the process of producing the TFT, before the formation of the source and drain electrodes 5, 6 an insulator film 9 is formed by the patterning of an insulator film deposited on the semiconductor layer 4. However, even in this type of TFT, the abovemen-

tioned problems (3) and (4) still remain to be solved. That is, in order to realize good TFT characteristics, it is necessary to reduce the stray capacity between the gate electrode and the source and drain electrodes. Furthermore, when a plurality of TFT are used as addressing devices in a liquid crystal display apparatus of the matrix type, it is required to increase the A/D ratio in order to improve the brightness and the contrast of a picture to be displayed.

Summary of the invention

An object of the present invention is to provide a reliable and stable TFT having a structure wherein the stray capacity between the gate electrode and the source and drain electrodes is reduced to result in good dynamic characteristics and the deterioration of the semiconductor layer does not occur in the process of producing a TFT.

Another object of the present invention is to provide a liquid crystal display having a large A/D ratio in which TFT's are used for addressing devices which has a large A/D ratio.

In accordance with the present invention, there is provided a new TFT comprising,

an insulating substrate;

a gate electrode formed on the insulating substrate;

a gate-insulating layer formed on the gate electrode;

a semiconductor layer formed on the gate-insulating layer;

an insulating layer formed so as to cover the semiconductor layer; and which has two openings;

a source electrode and a drain electrode formed on the insulating layer, wherein the source and drain electrodes are electrically contacted to the semiconductor layer through the said openings in the insulating layer.

Brief description of the drawings

Other objects and advantages of the invention will be apparent from the following description, the appending claims and accompanying drawings, in which:

Figure 1 is a schematic cross-sectional view of a prior-art TFT;

Figure 2 is a schematic cross-sectional view of another prior-art TFT;

Figure 3 is a schematic plan view of a part of a liquid crystal display wherein a prior-art TFT is used as an addressing device;

Figure 4 is a schematic cross-sectional view of a modified prior-art TFT;

Figures 5, 6 and *7* are each cross-sectional view of an embodiment of the present invention; and

Figure 8 is a schematic plan view of a part of a liquid crystal display of the active matrix display type.

Embodiments

Figure 5 shows a cross-section of TFT of an embodiment of the present invention. After a Ta film is deposited on a glass substrate 10 with a process such as vacuum deposition and sputtering, a gate electrode 20 of Ta is formed by etching away the unnecessary part of the Ta film with a patterning process. Next, a gate-insulating film 30 of Ta_2O_5 is formed on the surface of the gate electrode 20 by the anodic oxidation. A Si_3N_4 film and an a-Si film are successively deposited on the Ta_2O_5 film 30 and the glass substrate 10. Then, a double layer structure of a Si_3N_4 film 31 and an a-Si film 40 is formed so as to cover the Ta_2O_5 film 30 with a patterning process. Both Ta_2O_5 film 30 and Si_3N_4 film 31 compose a gate-insulating layer, and their thickness should be thin enough to obtain necessary TFT characteristics. The Si_3N_4 layer 31 is used to improve the gate-insulating properties of the Ta_2O_5 film 30. The a-Si film 40 is the semiconductor layer of TFT. Next, a Si_3N_4 film 90 is deposited so as to cover the semiconductor layer 40 with the plasma CVD process and slots 91 and 92 for the connection of a source electrode 50 and of a drain electrode 60 are dug through the Si_3N_4 film 90 with a patterning process near the edge of the gate electrode 20. Then, an Al film is deposited on the Si_3N_4 film 90 in the slots 91 and 92, and is separated to form a source electrode 50 and a drain electrode 60 of Al by a patterning process. Both electrodes 50, 60 are kept in contact with the a-Si film 40 through the slots 91 and 92 in the Si_3N_4 film 90 respectively. Next, a Si_3N_4 passivation film 70 is deposited with the plasma CVD process on the source electrode 50, the drain electrode 60 and the Si_3N_4 layer 90. Finally, an Al film is deposited on the Si_3N_4 passivation film 70, and a light shield 80 is formed by the patterning of the Al film. In a TFT thus produced, insulating layer of the Si_3N_4 film 90 is interposed between the a-Si semiconductor layer 40 and the source and drain electrodes 50, 60. It should be noted that the insulating layer 90 extends to almost all area of the semiconductor layer 40 except the slots 91 and 92.

As mentioned above, the source and drain electrodes 50, 60 of Al film keep in contact with the a-Si semiconductor layer 40 only through the slots 91 and 92 dug in the Si_3N_4 layer 90. That is, they do not keep unnecessary direct contact with the a-Si semiconductor layer 40 so that a portion of the latter 40 between the formers 50, 60 is not contaminated with Al impurities contained in the formers 50, 60 during the deposition process of Al film. Then, the temperature of the substrate 10 can be made high enough on the process of depositing an Al film to allow good contact of the a-Si semiconductor layer 40 and the source and drain electrodes 50, 60 in the slots 91 and 92. Furthermore, the stray capacity between the gate electrode 20 and the source and drain electrodes 50, 60 decreases because of the interposition of the insulating film 90.

Figure 6 shows a cross-section of a TFT of another embodiment of the present invention. The production process of the TFT is almost the same as that mentioned above except the following. The distance between the source and drain electrodes 50, 60 is shortened so that both electordes 50, 60 play a role as a light shield. Then, the process of forming the light shield 80 of Al film can be omitted.

Figure 7 shows a cross-section of a TFT of a third embodiment of the present invention. The produc-

tion process of the TFT is almost the same as that of a first embodiment except the process of forming the source and drain electrodes 50, 60. On the Si_3N_4 film 90 and the slots 91, 92, n^+ a-Si film is deposited with the plasma CVD process and next a Ti film with the vacuum deposition process. Then a source electrode of a double layer of n^+ a-Si 55 and of Ti 50 and drain electrode of n^+ a-Si 65 and of Ti 60 are formed with the patterning process. In the production process, the n^+ a-Si layer can be etched selectively so that the thickness of the a-Si semiconductor layer 90 can be made thinner.

When, TFT's according to the present invention are used as the addressing devices of a liquid crystal display apparatus of matrix type (Figure 8), it becomes unnecessary to make such wide gaps a and b as shown in Figure 3 between gate electrodes 2 and the pixel electrodes 100 because a thick insulating film 90 exists between them. Even the overlapping with each other does not cause troubles mentioned above. Then, the area of the pixel electrode can be made wider and the A/D ratio larger. Furthermore, the stray capacitance at the cross portions of the gate electrodes 20 with the source electrodes 50 can be reduced considerably because the thick gate-insulating film 90 is imterposed at the cross portions.

Obvious changes may be made in the specific embodiments described herein. For example, a TFT having similar characteristics to those of the abovementioned embodiments can be produced by using microcrystalline silicon for the semiconductor film 40. Such modifications being within the spirit and scope of the invention claimed, it is indicated that all matter contained herein is intended as an illustrative and not as limiting in scope.

CLAIMS

1. A thin film transistor comprising,
an insulating substrate;
a gate electrode formed on the insulating substrate;
a gate-insulating layer formed on the gate electrode;
a semiconductor layer formed on the gate-insulating layer;
an insulating layer formed so as to cover the semiconductor layer; and which has two openings;
a source electrode and a drain electrode formed on the insulating layer, wherein the source and drain electrodes are electrically contacted to the semiconductor layer through the openings in the insulating layer.

2. A thin film transistor according to Claim 1, wherein said semiconductor film is made of amorphous silicon.

3. A thin film transistor according to Claim 1, wherein said semiconductor film is made of microcrystalline silicon.

4. A thin film transistor according to Claim 1, wherein each of said openings of said insulating layer has narrow area for said source or drain electrodes to keep contact with said semiconductor layer.

5. A thin film transistor according to Claim 1, wherein said insulating layer is thick enough to lessen the stray capacity between said semiconductor layer and said source or drain electrodes.

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